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(54) **Distortion correction circuit**

Verzerrungskorrektionsschaltung

Circuit de correction de distorsion

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Description

Background of the Invention

Field of the Invention:

[0001] The present invention relates to a distortion correction circuit which is mounted on a television receiver or the like to correct image distortion.

Description of the Related Art:

[0002] Conventionally, a raster on a fluorescent screen showed pincushion distortion in the deflection process of a color television receiver because the radius of curvature of a fluorescent screen is longer than the axial length from a deflection center to a fluorescent screen. This distortion is called pincushion distortion. Even though a uniform pincushion correction is applied to the entire screen, pincushion distortion still remains in the center part (hereinafter called inner pincushion distortion) because of the difference of distortion degree between the peripheral part and the center part of the screen. Such inner pincushion distortion which is a shrinkage in the center part is caused by the difference of a horizontal linearity between the upper/lower parts and the center part of the screen.

[0003] Fig. 7 shows a distortion correction circuit of voltage modulation type called a diode modulator circuit. A diode modulator circuit of negative system will be described below. In this circuit, distortion is corrected by using the negative potential at a point C.

[0004] In Fig. 7, pulses of the horizontal period are supplied to an input terminal 1 and supplied to the base of a horizontal output transistor Q1. A damper diode D1 is connected in parallel between the collector and the emitter of the horizontal output transistor Q1 so that the cathode of the former is connected with the collector of the latter. In addition, a resonant capacitor C2 is connected in parallel with the horizontal output transistor Q1. Furthermore, the combination of a horizontal deflection coil Ly, a linearity coil L1 and a damping resistor R1 which are connected in parallel with each other, and S-shape correction capacitors C4 and C5 serially connected are connected in parallel with that transistor Q1.

[0005] The collector of the horizontal output transistor Q1 is connected with a power supply terminal 2 through the primary winding T1 of a flayback transformer FBT so as to supply the power supply voltage VB. Additionally, a resonant capacitor C1 is connected between the collector of the horizontal output transistor Q1 and the reference potential point.

[0006] The emitter of the horizontal output transistor Q1 is connected with the reference potential point via a parallel circuit of a modulation diode D2 and a resonant capacitor C3, and at the same time via a modulation coil L3 and a modulation capacitor C6. A joint A between the S-shape correction capacitors C4 and C5 is connected with the reference potential point via a coil L2.

[0007] A joint B of the modulation coil L3 and the modulation capacitor C6 is connected with the reference potential point via a resistor R2 and the collector-emitter path of the transistor Q2. A parabolic wave generating circuit (not shown) which generates the parabolic wave voltage of the vertical period is connected with a terminal 3 which is connected with the base of the transistor Q2.

[0008] The above-mentioned circuit is a horizontal output circuit in which the damper diode D1 and the resonant capacitor C2 are connected in parallel with the horizontal output transistor Q1. In addition, in this circuit, a distortion correction circuit is connected with the peripheral part of the S-shape correction capacitors C4 and C5. The S-shape capacitor is divided into C4 and C5. A coil L2 is connected between the joint A of these capacitors C4 and C5 and the reference potential point. For the purpose of distortion correction, a distortion correction circuit consisting of a series circuit of the coil L3 and the capacitor C6 as well as the resonant capacitor C3 is connected in parallel between one terminal of the S-shape correction capacitor C5 (the emitter of Q1) and the reference potential point. The diode D2 maintains the negative voltage generated at the emitter of the transistor Q1 and guarantees the operation of the horizontal output transistor Q1.

[0009] In the horizontal scanning period, the horizontal deflection current flows through the horizontal output transistor Q1 or the damper diode D1. The current I1 flows from the S-shape correction capacitor C5 through the coil L2. The charge stored in the S-shape correction capacitors C4 and C5 flows to the horizontal deflection coil Ly through the coil L1 as a horizontal deflection current Iy. Only the horizontal deflection current Iy flows through the S-shape correction capacitor C4 on the horizontal deflection coil side. Both I1 and Iy flow through the S-shape correction capacitor C5. The parabolic wave voltage of the vertical period is applied to the terminal 3 connected with the base of the transistor Q2 to modulate the terminal voltage Vm of the capacitor 6 parabolically. When the voltage Vm of the capacitor C6 is modulated parabolically with the vertical period, the S-shape capacitor voltage (Vc5+Vc4) as the power source of the horizontal deflection current Iy is modulated as expressed by Vc5+Vc4=VB+Vm. In the above equation, Vc5 is the voltage across the S-shape correction capacitor C5, and Vc4 is the voltage across the S-shape correction capacitor C4. In this case, the capacity of the S-shape correction capacitor is set as C5<<C4, so Vc4 can be disregarded. That is, Vc5 is modulated parabolically with the vertical period by modulating Vm. Therefore, as shown in Fig. 8, the voltage of the horizontal period Vc5 modulated parabolically with the vertical period appears across the S-shape correction capacitor C5.

[0010] By using the voltage waveform modulated parabolically with the vertical period, inner pincushion distortion which occurs different horizontal linearities in the

upper/lower and the center parts of the screen and occurs a shrinkage in the center part of the screen, is corrected to a uniform pincushion distortion as shown with the dotted line and the solid line in Fig. 9 (a). Such corrected pincushion distortion is further corrected as shown in Fig. 9 (b) by adjusting the parabolic wave by a DPC (Dynamic Pincushion Correction) circuit.

[0011] Fig. 10 shows the circuit diagram of a diode modulator circuit of positive system. Compared with the diode modulator circuit of the negative system shown in Fig. 7, the emitter of the horizontal output transistor Q1 is connected with the reference potential point and the diode D2 is connected serially in the same direction as that of the damper diode D1. In this circuit, the resonant capacitor C1 is removed between the collector of the horizontal output transistor Q1 and the reference potential point. In the circuit shown in Fig. 7, distortion is corrected by using the negative potential at the point C, but in the circuit shown in Fig. 10, such correction is performed by using the positive voltage at the point C.

[0012] However, the circuits shown in Fig. 7 or 10 are disadvantageous in the substrate area and the cost, because large parts such as coils and capacitors are employed. In addition, each time the inductance of a deflection yoke and the curvature of a picture tube change due to the model change, it is necessary to redesign the part constants, which is troublesome.

[0013] EP-A2-0,589,512 describes an image distortion correction circuit which stores incoming video signal data in a memory and controls the rate at which the data is read from the memory. This is controlled by a correction circuit which receives a line deflection reference signal which is delayed so as to try to align the deflection signals with the incoming video signals.

[0014] US-5,041,764 describes an apparatus which amongst other things can be used for correcting pin cushion distortion. This document similarly describes storing incoming video signal data in a memory and controlling the reading of the data from that memory to provide the signal provided to the screen. The control of the reading rate from the memory is achieved by modulating the pixel clock frequency at the center of the screen relative to that at the right and left sides of the screen for one horizontal scanning line.

Summary of the Invention

[0015] It is an object of the present invention to provide a distortion correction circuit which can correct the distortion of an image on the screen without performing the troublesome calculation of the constants of newly adopted parts.

[0016] According to a first aspect of the present invention there is provided a distortion correction circuit for correcting inner pin cushion distortion occuring on a screen, comprising:

an analog-to-digital conversion means for receiving an analog luminance signal and analog color difference signals to convert them into the corresponding digital signals respectively;

a memory means for storing said signals subjected to the analog-to-digital conversion by said A/D conversion means; characterised by

a write/read controlling means 140 for controlling the write operations of signals for said memory means and for modulating the reading of data written in said memory means with both a horizontal period and a vertical period so as to enable the reading; and

a digital-to-analog conversion means for converting the signals read out of said memory means into an analog luminance signal and analog color difference signals;

wherein said write/read controlling means includes parabolic wave generation circuits for generating parabolic waves varying with a horizontal period and with a vertical period and said write-read controlling means is adapted to parabolically modulate said reading speed in response to outputs from said parabolic wave generation circuits such that the reading speed from said memory means during the vertical period is increased in the center part in the vertical direction of the screen and decreased at the upper and lower parts of the screen, the reading speed from said memory means during the horizontal period is decreased in the center part in the horizontal direction of the screen and increased at the right and left parts of the screen, and the reading speed at said right and left parts of the screen is higher in the center part of the screen than that in the upper and lower parts in the vertical direction of the screen.

[0017] The present invention further provides a distortion correction circuit for correcting inner barrel distortion occuring on a screen, comprising:

an analog-to-digital conversion means for receiving an analog luminance signal and analog color difference signals to convert them into the corresponding digital signals respectively;

a memory means for storing said signals subjected to the analog-to-digital conversion by said A/D conversion means; characterised by

a write/read controlling means 140 for controlling the write operations of signals for said memory means and for modulating the reading of data written in said memory means with both a horizontal period and a vertical period so as to enable the reading; and

a digital-to-analog conversion means for converting the signals read out of said memory means into an analog luminance signal and analog color difference signals;

wherein said write/read controlling means (140) in-

cludes parabolic wave generation circuits (117, 118) for generating parabolic waves varying with horizontal period and with a vertical period and said write/read controlling means is adapted to parabolically modulate said reading speed in response to outputs from said parabolic wave generation circuits, such that the reading speed from said memory means during the vertical period is decreased in the center part in the vertical direction of the screen and increased at the upper and lower parts of the screen, the reading speed from said memory means during the horizontal period is decreased in the center part in the horizontal direction of the screen and increased at the right and left parts of the screen, and the reading speed at said right and left parts of the screen is slower in the center part of the screen than that in the upper and lower parts in the vertical direction of the screen.

[0018] The luminance signal and the color difference signals after the A/D conversion are stored in the memory means once. When reading such stored signal out of the memory means, reading speed is modulated parabolically with both the horizontal period and the vertical period. Such a modulated digital signal is subjected to the D/A conversion to obtain an analog luminance signal and an analog color difference signals and the inner pincushion distortion or the inner barrel distortion is corrected. That is, distortion can be corrected by modulating the image signal itself by digital processing, so circuit drift due to the conventional analog correction does not occur and no complicated analog circuit design is required.

[0019] In the above-mentioned write/read controlling means in the distortion correction circuit there may be provided:

a clock generating circuit for generating a first timing signal, a first write clock having a frequency of a predetermined multiple of a horizontal scanning frequency and a second clock having a frequency of a predetermined multiple different from the above multiple of the horizontal scanning frequency on the basis of the horizontal synchronizing signal;
a digital control oscillator for generating a clock, on the basis of the second clock above described, whose oscillation frequency is parabolically modulated with both horizontal period and vertical period;
a horizontal parabolic wave generating circuit for generating a parabolic wave signal of the horizontal period on the basis of the horizontal synchronizing signal and supplying that signal to the digital control oscillator;
a vertical parabolic wave generating circuit for generating a parabolic wave signal of the vertical period on the basis of the vertical synchronizing signal and supplying that signal to the digital control oscillator;
a digital-to-analog converter which converts the output of the digital control oscillator into an analog signal and outputs that signal to the memory means as a read clock;
a timing generating circuit for generating a write timing signal on the basis of the first timing signal and the first clock, and also generating a read timing signal on the basis of the first timing signal and the read clock from the D/A converter.

[0020] In the above a read clock is generated digitally in the digital control oscillator and a read clock frequency can be parabolically and precisely modulated with both horizontal period and vertical period.

Brief Description of the Drawings:

[0021] Fig. 1 is a block diagram showing the distortion correction circuit of an embodiment according to the present invention.

[0022] Fig. 2 is a block diagram showing the configuration of a display apparatus in which the distortion correction circuit of Fig. 1 is used.

[0023] Fig. 3 (a) is a diagram showing the modulation waveform of the reading speed during the vertical period (1V) for removing inner pincushion distortion in the line memory circuit of Fig. 1.

[0024] Fig. 3 (b) is a diagram showing the modulation waveform of the reading speed during the horizontal period (1H) for removing inner pincushion distortion in the line memory circuit of Fig. 1.

[0025] Figs. 4 (a) - (c) are diagrams for describing an inner pincushion distortion correction sequence in the circuit of Fig. 1.

[0026] Fig. 5 (a) is a diagram of the modulation waveform of the reading speed at 1V for removing inner barrel distortion in the line memory circuit of Fig. 1.

[0027] Fig. 5 (b) is a diagram of the modulation waveform of the reading speed at 1H for removing inner barrel distortion in the line memory circuit of Fig. 1.

[0028] Figs. 6 (a) - (c) are diagrams for describing an inner barrel distortion correction sequence in the circuit of Fig. 1.

[0029] Fig. 7 is a circuit diagram of the conventional distortion correction circuit of diode modulator system of negative type

[0030] Fig. 8 is a diagram showing the correction voltage waveform in the circuit of Fig. 7.

[0031] Figs. 9 (a) and (b) are diagrams for describing an inner pincushion distortion correction sequence in the circuit of Fig. 7.

[0032] Fig. 10 is a circuit diagram of the conventional distortion correction circuit of diode modulator system of positive type.

Detailed Description of the Preferred Embodiments

[0033] The preferred embodiments of the present invention will be described below with reference to the

drawings.

[0034] Fig. 1 is a block diagram showing the distortion correction circuit of an embodiment of the present invention. Fig. 2 is a block diagram of the display apparatus such as a television receiver in which the distortion correction circuit of Fig. 1 is used. First, the display apparatus of Fig. 2 will be described below.

[0035] In Fig. 2, the display apparatus comprises a distortion correction circuit 100, a video output circuit 200, a deflection circuit 300 and a cathode ray tube (CRT) 400.

[0036] The analog luminance signal Y and the analog color difference signals R-Y and B-Y are applied to the distortion correction circuit 100. These signals are respectively converted into the corresponding digital signals. Then the resulting signals are written in the memory means. When these signals are read from the memory means, the reading speed of the Y, R-Y and the B-Y signals are modulated parabolically with both horizontal period (hereinafter called 1H) and vertical period (hereinafter called 1V) according to the signal based on the horizontal synchronizing signal HD and the vertical synchronizing signal VD. They are converted again into the analog luminance signal Y and the color difference signals R-Y and B-Y and outputted therefrom.

[0037] The luminance signal Y and the color difference signals R-Y and B-Y from the distortion correction circuit 100 are applied to the video output circuit 200. The video output circuit supplies three primary color signals, a red (R) signal, a green (G) signal and a blue (B) signal to the CRT 400.

[0038] The horizontal synchronizing signal HD and the vertical synchronizing signal above-mentioned are applied to the deflection circuit 300. This circuit supplies the horizontal deflection current and the vertical deflection current to the deflection yoke of the cathode ray tube (CRT) 400. It includes a DPC (Dynamic Pincushion Correction) circuit.

[0039] In Fig. 1, the analog luminance signal Y is applied to the input terminal 101. That signal is converted into a digital luminance signal 103 in the A/D converter 102. This digital luminance signal is applied to the line memory circuit 128 as a memory means. The analog color difference signals R-Y and B-Y are respectively applied to the input terminals 104, 105. These signals are supplied to the A/D converter 108. In this converter, they are multiplexed each other and converted into a digital chrominance signal 109 and supplied to the line memory circuit 128.

[0040] The digital signal is written in the line memory circuit 128 by using the write clock 113 from the clock generating circuit 111 according to the write timing signal 126 from the timing circuit 125.

[0041] The horizontal synchronizing signal HD is applied to the input terminal 110, then to the clock generating circuit 111. The clock generating circuit 111 generates the timing signal 112 for the write/read timing, a 910fH clock (113) having a frequency of 910 times as high as the horizontal scanning frequency fH, and a 2730fH clock (114) having a frequency 2730 times as high as the horizontal scanning frequency fH.

[0042] The timing signal 112 is applied to the timing generating circuit 125. The 910fH clock (113) is applied to the line memory circuit 128 as the write clock, and at the same time to the timing generating circuit 125. The timing circuit 125 generates a write timing signal 126 synchronized with the 910fH clock (113), using the timing signal 112 and the above-mentioned 910fH clock (113) and supplies it to the line memory circuit 128.

[0043] The 2730fH clock (114) is applied to the digital control oscillator 115. The digital control oscillator 115 generates a read clock in a digital manner on the basis of the 2730fH clock (114). It has the function to modulate the read clock frequency, namely, the reading speed with 1H and 1V, using the horizontal parabolic wave signal 141 from the horizontal parabolic wave generating circuit 117 and the vertical parabolic wave signal 142 from the vertical parabolic wave generating circuit 118.

[0044] The horizontal parabolic wave generating circuit 117 generates the parabolic wave signal 141 of 1H on the basis of the horizontal synchronizing signal HD supplied to the input terminal 110 and supplies it to the digital control oscillator 115 as a control signal. The vertical parabolic wave generating circuit 118 generates the parabolic wave signal 142 of 1V on the basis of the vertical synchronizing signal VD supplied to the input terminal 116 and supplies it to the digital control oscillator 115 as a control signal. The digital clock signal 120 speed-modulated parabolically with 1H and 1D to be outputted from the digital control oscillator 115 is converted into an analog clock signal 122 in the D/A converter 121. The waveform of the resulting signal is shaped in the waveform shaping circuit 123 and supplied to the line memory circuit 128 as a reading clock 124 and to the above-mentioned timing generating circuit 125. The timing generating circuit 125 generates a read timing clock 127 synchronized with the read clock 124, using the timing signal 112 and the read clock 124 and supplies it to the line memory circuit 128. The circuit portion in the dotted line frame 140 is the write/read controlling means.

[0045] In the line memory circuit 128, the reading speed of the digital luminance signal Y and the digital color difference signals R-Y and B-Y stored therein are modulated and read as signals 129, 130. The digital luminance signal 129 is supplied to the D/A converter 131, and the digital chrominance signal 130 is supplied to the D/A converters 133, 134

[0046] The D/A converter 131 converts the digital luminance signal into the analog luminance signal Y and outputs it from the output terminal 132. The D/A converter 133 separates the digital color difference signal R-Y from the multiplexed digital chrominance signal 130, converts the separated signal into the analog color difference signal R-Y and outputs it from the output terminal 135. The D/A converter 134 separates the digital

color difference signal B-Y from the multiplexed digital chrominance signal 130, converts the separated signal into the analog color difference signal B-Y and outputs it from the output terminal 136.

[0047] The operation shown in Fig. 1, especially the operation for correcting inner pincushion distortion shown in Fig.4 (a) will be described below with reference to Figs. 3 (a) and (b) and Figs. 4 (a) - (c).

[0048] The analog luminance signal Y and the analog color difference signals R-Y and B-Y are applied to the input terminals 101, 104 and 105. The horizontal synchronizing signal HD and the vertical synchronizing signal VD are applied to the input terminals 110, 116. The analog luminance signal Y and the color difference signals R-Y and B-Y are respectively converted into the corresponding digital signals in the A/D converter 102, 108. The resulting signals are written in the line memory circuit 128. Such signals are written according to the write timing signal 126 from the timing generating circuit 125 and the write clock 113 from the clock generating circuit 111. The write clock 113 is a clock having the constant frequency of 910fH.

[0049] In the read operation, the digital control oscillator 115 generates a digital read clock 120 according to a clock 114 having the frequency of 2730fH. In this case, the frequency of the generated signal (namely, the reading frequency) is modulated with 1H and 1V, using the parabolic wave signal 141 of 1H from the horizontal parabolic wave generating circuit 117 and the parabolic wave signal 142 of 1V from the vertical parabolic wave generating circuit 118 as control signals. The resulting digital clock signal 120 is converted into an analog signal 122 in the D/A converter 121. The waveform of the converted signal is shaped in the waveform shaping circuit 123 and supplied to the line memory circuit 128 as the read clock 124. When the digital luminance signal and the digital chrominance signal stored in the line memory circuit 128 are read from the line memory circuit 128, the reading speed of the digital luminance signal and the digital chrominance signal is parabolically modulated with 1H and 1V according to the read clock 124.

[0050] Fig. 3(a) shows the modulation waveform of the reading speed at 1V. Fig. 3(b) shows the modulation waveform of the reading speed at 1H. To correct inner pincushion distortion, as shown in Fig. 3(a), it is necessary to increase the modulating speed in the horizontal direction in the center part of the screen during 1V and to decrease the modulating speed in the upper and lower parts of the screen. At the same time, as shown in Fig. 3(b), it is also necessary to slow down the modulating speed in the center part of the screen during 1H and to speed up such speed in the right and left parts of the screen. As shown in Fig. 3(b), it is also necessary to change the modulating speed regarding the period of 1H in the center part of the screen during 1V and in the upper and lower parts of the screen. That is, as shown in Fig. 3(b), the modulating speed on the scanning lines in the center part is higher than that on the scanning lines in the upper and lower parts at the right and left parts of the screen. That is, the modulating speed on the scanning lines in the upper and lower parts of the screen is slower than that on the scanning lines in the center part at the right and left parts of the screen.

[0051] The digital luminance signal and the digital chrominance signal read out of the line memory circuit 128 are again converted into an analog luminance signal Y and analog color difference signals R-Y and B-Y in the D/A converters 131, 133, and 134. The resulting signals are applied to the video output circuit (200 in Fig. 2) (not shown in this fig.) and displayed on the CRT.

[0052] Using the 1V and 1H reading speed modulation means by the line memory circuit 128 as descnbed above, the distortion of an image to be displayed on the CRT is corrected as shown in Fig. 4 (c). That is, if no distortion correction is made, an image to be displayed has inner pincushion distortion as shown in Fig. 4 (a). Such distortion is corrected to uniform pincushion distortion as shown in Fig. 4 (b) by means of the distortion correction circuit 100 of the present embodiment. Moreover, by correcting pincushion distortion by means of the DPC circuit in the deflection circuit 300 additionally, an image which is completely free from pincushion distortion is displayed on the CRT as shown in Fig. 4 (c).

[0053] The correction procedure of an inner barrel distortion as shown in Fig. 6 (a) will be described below with reference to Figs. 5 (a) and (b) as well as Figs. 6 (a) - (c).

[0054] If inner barrel distortion occurs under the condition where no distortion correction is made, such distortion can be corrected by inverting the polarity of the modulation waveform of the reading speed as shown in Fig. 3(a) into the polarity as shown in Fig. 5(a).

[0055] Fig. 5(a) shows the modulation waveform of the reading speed at 1V. Fig. 5 (b) shows the modulation waveform of the reading speed at 1H. To correct inner barrel distortion, as shown in Fig. 5 (a), it is necessary to slow down the modulating speed in the horizontal direction in the center part at 1V on the screen and to speed up the modulating speed in the upper and lower parts of the screen. On the other hand, as shown in Fig. 5 (b), it is necessary to slow down the modulating speed in the center part at 1H on the screen and to speed up it in the right and left parts of the screen. It is also necessary, as shown in Fig. 5 (b), to change the modulating speed regarding the period of 1H in the center part at 1V on the screen and in the upper and lower parts on the screen. That is, as shown in Fig. 5 (b), it is necessary to decrease the modulating speed on the scanning lines in the center part to become slower than that on the scanning lines in the upper and lower parts at the right and left parts of the screen. In other words, it is necessary to increase the modulating speed on the scanning lines in the upper and lower parts to become faster than that on the scanning lines in the center part at the right and left parts of the screen.

[0056] Using the 1V and 1H reading speed modula-

tion means by the line memory circuit 128 as described above, the distortion of an image to be displayed on the CRT is corrected as shown in Fig. 6 (c). That is, if no distortion correction is made, an image to be displayed has inner barrel distortion as shown in Fig. 6 (a). Such distortion is corrected to uniform barrel distortion as shown in Fig. 6 (b) by means of the distortion correction circuit 100 of the present embodiment. Moreover, by correcting the barrel distortion by means of the DPC circuit in the deflection circuit 300 additionally, an image which is free from barrel distortion is displayed on the CRT as shown in Fig. 6 (c).

[0057] As described above, according to the present invention, the conventional analog correction of inner pincushion distortion or inner barrel distortion by a deflection circuit can be digitally corrected by modulating an image signal itself. As a result, no circuit drift due to the conventional analog correction occurs and no complicated analog circuit design is required.

[0058] The present invention is not limited to the above-mentioned embodiments, but various changes and modifications can be made without departing from the scope of the present invention.

Claims

1. A distortion correction circuit for correcting inner pincushion distortion occuring on a screen, comprising:

   an analog-to-digital (A/D) conversion means (102, 108) for receiving an analog luminance signal and analog color difference signals to convert them into the corresponding digital signals respectively;
   a memory means (128) for storing said signals subjected to the analog-to-digital conversion by said A/D conversion means (102, 108);
   a write/read controlling means 140 for controlling the write operation of signals for said memory means (128) and for modulating the reading speed of data written in said memory means; and
   a digital-to-analog (D/A) conversion means (131, 133 and 134) for converting the signals read out of said memory means (128) into an analog luminance signal and analog color difference signals; characterised in that
   said write/read controlling means (140) includes parabolic wave generation circuits (117, 118) for generating parabolic waves varying with a horizontal period and with a vertical period and said write-read controlling means is adapted to parabolically modulate said reading speed in response to outputs from said parabolic wave generation circuits such that the reading speed from said memory means during the vertical period is increased in the center part in the vertical direction of the screen and decreased at the upper and lower parts of the screen, the reading speed from said memory means during the horizontal period is decreased in the center part in the horizontal direction of the screen and increased at the right and left parts of the screen, and the reading speed at said right and left parts of the screen is higher in the center part of the screen than that in the upper and lower parts in the vertical direction of the screen.

2. A distortion correction circuit for correcting inner barrel distortion occuring on a screen comprising:

   an analog-to-digital (A/D) conversion means (102, 108) for receiving an analog luminance signal and analog color difference signals to convert them into the corresponding digital signals respectively;
   a memory means (128) for storing said signals subjected to the analog-to-digital conversion by said A/D conversion means (102, 108);
   a write/read controlling means 140 for controlling the write operations of signals for said memory means (128) and for modulating the reading of data written in said memory means; and
   a digital-to-analog (D/A) conversion means (131, 133 and 134) for converting the signals read out of said memory means (128) into an analog luminance signal and analog color difference signals; characterised in that
   said write/read controlling means (140) includes parabolic wave generation circuits (117, 118) for generating parabolic waves varying with a horizontal period and with a vertical period and said write/read controlling means is adapted to parabolically modulate said reading speed in response to outputs from said parabolic wave generation circuits, such that the reading speed from said memory means during the vertical period is decreased in the center part in the vertical direction of the screen and increased at the upper and lower parts of the screen, the reading speed from said memory means during the horizontal period is decreased in the center part in the horizontal direction of the screen and increased at the right and left parts of the screen, and the reading speed at said right and left parts of the screen is slower in the center part of the screen than that in the upper and lower parts in the vertical direction of the screen.

3. A write/read controlling means (111, 115, 117, 118, 121, and 125) in the distortion correction circuit ac-

cording to claim 1 or 2, comprising :

a clock generating circuit (111) for generating a first timing signal (112), a first write clock (113) having a frequency of a predetermined multiple of a horizontal scanning frequency and a second clock (114) having a frequency of a predetermined multiple different from the above multiple of the horizontal scanning frequency on the basis of the horizontal synchronizing signal;
a digital control oscillator (115) for generating a clock (120), on the basis of said second clock (114), whose oscillation frequency is parabolically modulated with both horizontal period and vertical period;
a horizontal parabolic wave generating circuit (117) for generating the parabolic wave signal (141) of the horizontal period on the basis of said horizontal synchronizing signal and supplying the signal to said digital control oscillator (115);
a vertical parabolic wave generating circuit (118) for generating the parabolic wave signal (142) of the vertical period on the basis of said vertical synchronizing signal and supplying the signal to said digital control oscillator (115);
a digital-to-analog converter (121) for converting the output of said digital control oscillator (115) into an analog signal and outputting that signal to said memory means (128) as a read clock (122); and
a timing generating circuit (125) for generating a write timing signal (126) on the basis of said first timing signal (112) and said first write clock (113), and also generating a read timing signal (127) on the basis of said first timing signal (112) and a read clock (122) from said digital-to-analog converter (121).

Patentansprüche

1. Verzerrungskorrekturschaltung zum Korrigieren einer inneren Nadelkissenverzerrung, die auf einem Schirm auftritt, aufweisend:

eine Analog/Digital- (A/D-) Umwandlungseinrichtung (102, 108) zum Empfangen eines analogen Luminanzsignals und analoger Farbdifferenzsignale zur Umwandlung derselben in die jeweils entsprechenden Digitalsignale;

eine Speichereinrichtung (128) zum Speichern der Signale, die der Analog/Digital-Umwandlung durch die A/D-Umwandlungseinrichtung (102, 108) unterworfen sind;

eine Schreib/Lese-Steuereinrichtung (140) zum Steuern der Schreiboperationen von Signalen für die Speichereinrichtung (128) und zum Modulieren der Lesegeschwindigkeit von in die Speichereinrichtung geschriebenen Daten; und

eine Digital-/Analog- (D/A-) Umwandlungseinrichtung (131, 133 und 134) zur Umwandlung der aus der Speichereinrichtung (128) ausgelesenen Signale in ein analoges Luminanzsignal und analoge Farbdifferenzsignale;

dadurch gekennzeichnet, daß:
die Schreib/Lese-Steuereinrichtung (140) Erzeugungsschaltungen (117, 118) für Parabolwellen zum Erzeugen von Parabolwellen, die mit einer horizontalen Periode und mit einer vertikalen Periode variieren, einschließen und daß die Schreib/Lese-Steuereinrichtung ausgelegt ist, die Lesegeschwindigkeit in Antwort auf die Ausgänge von den Erzeugungsschaltungen für Parabolwellen derart parabolisch zu modulieren, daß die Lesegeschwindigkeit von der Speichereinrichtung während der vertikalen Periode in dem zentralen Teil der vertikalen Richtung des Schirms erhöht wird und an den oberen und unteren Teilen des Schirms verringert wird, die Lesegeschwindigkeit von der Speichereinrichtung während der horizontalen Periode in dem zentralen Teil in der horizontalen Richtung des Schirms verringert wird und an den linken und rechten Teilen des Schirms erhöht wird und die Lesegeschwindigkeit an den rechten und linken Teilen des Schirms höher im zentralen Teil des Schirms als in den oberen und unteren Teilen in der vertikalen Richtung des Schirms ist.

2. Verzerrungskorrekturschaltung zum Korrigieren einer inneren Tonnenverzerrung, die aufeinem Schirm auftritt, aufweisend:

eine Analog/Digital- (A/D-) Umwandlungseinrichtung (102, 108) zum Empfangen eines analogen Luminanzsignals und analoger Farbdifferenzsignale zur Umwandlung derselben in die jeweils entsprechenden digitalen Signale;

eine Speichereinrichtung (128) zum Speichern der Signale, die der Analog/Digital-Umwandlung durch die A/D-Umwandlungseinrichtung (102, 108) unterworfen sind;

eine Schreib/Lese-Steuereinrichtung (140) zum Steuern der Schreiboperationen von Signalen für die Speichereinrichtung (128) und zum Modulieren des Lesens von in die Speichereinrichtung geschriebenen Daten; und

eine Digital/Analog- (D/A-) Umwandlungsein-

richtung (131, 133 und 134) zur Umwandlung der aus der Speichereinrichtung (128) ausgelesenen Signale in ein analoges Luminanzsignal und analoge Farbdifferenzsignale;

dadurch gekennzeichnet, daß:

die Schreib/Lese-Steuereinrichtung (140) Erzeugungsschaltungen (117, 118) für Parabolwellen zum Erzeugen von Parabolwellen, die mit einer horizontalen Periode und mit einer vertikalen Periode variieren, einschließt und die Schreib/Lese-Steuereinrichtung ausgelegt ist, die Lesegeschwindigkeit in Antwort auf die Ausgänge der Erzeugungsschaltungen für Parabolwellen derart parabolisch zu modulieren, daß die Lesegeschwindigkeit von der Speichereinrichtung während der vertikalen Periode in dem zentralen Teil in der vertikalen Richtung des Schirms verringert wird und an den oberen und unteren Teilen des Schirms erhöht wird, die Lesegeschwindigkeit von der Speichereinrichtung während der horizontalen Periode in dem zentralen Teil in der horizontalen Richtung des Schirms verringert wird und an den rechten und linken Teilen des Schirms erhöht wird und die Lesegeschwindigkeit an den rechten und linken Teilen des Schirms langsamer in dem zentralen Teil des Schirms als jene in den oberen und unteren Teilen in der vertikalen Richtung des Schirms ist.

3. Schreib/Lese-Steuereinrichtung (111, 115, 117, 118, 121 und 125) in der Verzerrungskorrekturschaltung nach Anspruch 1 oder 2, aufweisend:

eine Takterzeugungsschaltung (111) zum Erzeugen eines ersten Zeitsignals (112), eines ersten Schreibtakts (113) mit einer Frequenz eines vorbestimmten Vielfachen einer horizontalen Scanfrequenz und eines zweiten Takts (114) mit einer Frequenz eines vorbestimmten Vielfachen, das verschieden von dem obigen Vielfachen der horizontalen Scanfrequenz ist, auf der Basis des horizontalen Synchronisiersignals;

einen digitalen Steueroszillator (115) zum Erzeugen eines Takts (120) auf der Basis des zweiten Takts (114), dessen Oszillationsfrequenz parabolisch sowohl mit der horizontalen Periode als auch mit der vertikalen Periode moduliert ist;

eine Erzeugungsschaltung (117) für horizontale Parabolwellen zum Erzeugen des Parabolwellensignals (141) der horizontalen Periode auf der Basis des horizontalen Synchronisiersignals und zum Zuführen des Signals zu dem digitalen Steueroszillator (115);

eine Erzeugungsschaltung (118) für vertikale Parabolwellen zum Erzeugen des Parabolwellensignals (142) der vertikalen Periode auf der Basis des vertikalen Synchronisiersignals und zum Zuführen des Signals zu dem digitalen Steueroszillator (115);

einen Digital/Analog-Wandler (121) zur Umwandlung des Ausgangs des digitalen Steueroszillators (115) in ein Analogsignal und zum Ausgeben jenes Signals zu der Speichereinrichtung (128) als ein Lesetakt (122); und

eine Zeitablauf-Erzeugungsschaltung (125) zum Erzeugen eines Schreibzeitsignals (126) auf der Basis des ersten Zeitsignals (112) und des ersten Schreibtakts (113), und auch zum Erzeugen eines Lesezeitsignals (127) auf der Basis des ersten Zeitsignals (112) und eines Lesetakts (122) von dem Digital/Analog-Wandler (121).

Revendications

1. Circuit de correction de distorsion pour corriger une distorsion en pelote à épingles interne survenant sur un écran, comprenant:

un moyen de conversion analogique-numérique (A/N) (102, 108) pour recevoir un signal de luminance analogique et des signaux de différence de couleur analogiques afin de les convertir respectivement selon les signaux numériques correspondants;

un moyen de mémoire (128) pour stocker lesdits signaux soumis à la conversion analogique-numérique par ledit moyen de conversion A/N (102, 108);

un moyen de commande d'écriture/lecture (140) pour commander l'opération d'écriture de signaux pour ledit moyen de mémoire (128) et pour moduler la vitesse de lecture de données écrites dans ledit moyen de mémoire; et

un moyen de conversion numérique-analogique (N/A) (131, 133 et 134) pour convertir les signaux lus dans ledit moyen de mémoire (128) selon un signal de luminance analogique et des signaux de différence de couleur analogiques,

caractérisé en ce que:

ledit moyen de commande d'écriture/lecture (140) inclut des circuits de génération d'onde parabolique (117, 118) pour générer des ondes paraboliques variant selon une période horizontale et se-

lon une période verticale et ledit moyen de commande d'écriture/lecture est adapté pour moduler de façon parabolique ladite vitesse de lecture en réponse à des sorties en provenance desdits circuits de génération d'onde parabolique de telle sorte que la vitesse de lecture dans ledit moyen de mémoire pendant la période verticale soit augmentée dans la partie centrale suivant la direction verticale de l'écran et soit diminuée au niveau des parties supérieure et inférieure de l'écran, que la vitesse de lecture dans ledit moyen de mémoire pendant la période horizontale soit diminuée dans la partie centrale suivant la direction horizontale de l'écran et soit augmentée au niveau des parties droite et gauche de l'écran et que la vitesse de lecture au niveau desdites parties droite et gauche de l'écran soit supérieure dans la partie centrale de l'écran à celles dans les parties supérieure et inférieure suivant la direction verticale de l'écran.

2. Circuit de correction de distorsion pour corriger une distorsion en tonneau interne survenant sur un écran, comprenant:

un moyen de conversion analogique-numérique (A/N) (102, 108) pour recevoir un signal de luminance analogique et des signaux de différence de couleur analogiques afin de les convertir respectivement selon les signaux numériques correspondants;

un moyen de mémoire (128) pour stocker lesdits signaux soumis à la conversion analogique-numérique par ledit moyen de conversion A/N (102, 108);

un moyen de commande d'écriture/lecture (140) pour commander les opérations d'écriture de signaux pour ledit moyen de mémoire (128) et pour moduler la lecture de données écrites dans ledit moyen de mémoire; et

un moyen de conversion numérique-analogique (N/A) (131, 133 et 134) pour convertir les signaux lus dans ledit moyen de mémoire (128) selon un signal de luminance analogique et des signaux de différence de couleur analogiques,

caractérisé en ce que:

ledit moyen de commande d'écriture/lecture (140) inclut des circuits de génération d'onde parabolique (117, 118) pour générer des ondes paraboliques variant selon une période horizontale et selon une période verticale et ledit moyen de commande d'écriture/lecture est adapté pour moduler de façon parabolique ladite vitesse de lecture en réponse à des sorties en provenance desdits circuits de génération d'onde parabolique de telle sorte que la vitesse de lecture dans ledit moyen de mémoire pendant la période verticale soit diminuée dans la partie centrale suivant la direction verticale de l'écran et soit augmentée au niveau des parties supérieure et inférieure de l'écran, que la vitesse de lecture dans ledit moyen de mémoire pendant la période horizontale soit diminuée dans la partie centrale suivant la direction horizontale de l'écran et soit augmentée au niveau des parties droite et gauche de l'écran et que la vitesse de lecture au niveau desdites parties droite et gauche de l'écran soit inférieure dans la partie centrale de l'écran à celles dans les parties supérieure et inférieure suivant la direction verticale de l'écran.

3. Moyen de commande d'écriture/lecture (111, 115, 117, 118, 121 et 125) dans le circuit de correction de distorsion selon la revendication 1 ou 2, comprenant:

un circuit de génération d'horloge (111) pour générer un premier signal de cadencement (112), une première horloge d'écriture (113) présentant une fréquence d'un multiple prédéterminé d'une fréquence de balayage horizontal et une seconde horloge (114) présentant une fréquence d'un multiple prédéterminé différent du multiple mentionné ci-avant de la fréquence de balayage horizontal sur la base du signal de synchronisation horizontale;

un oscillateur de commande numérique (115) pour générer une horloge (120), sur la base de ladite seconde horloge (114), dont une fréquence d'oscillation est modulée de façon parabolique suivant à la fois la période horizontale et la période verticale;

un circuit de génération d'onde parabolique horizontale (117) pour générer le signal d'onde parabolique (141) de la période horizontale sur la base dudit signal de synchronisation horizontale et pour appliquer le signal sur ledit oscillateur de commande numérique (115);

un circuit de génération d'onde parabolique verticale (118) pour générer le signal d'onde parabolique (142) de la période verticale sur la base dudit signal de synchronisation verticale et pour appliquer le signal sur ledit oscillateur de commande numérique (115);

un convertisseur numérique-analogique (121) pour convertir la sortie dudit oscillateur de commande numérique (115) selon un signal analogique et pour émettre en sortie ce signal sur ledit moyen de mémoire (128) en tant qu'horloge de lecture (122); et

un circuit de génération de cadencement (125) pour générer un signal de cadencement d'écriture (126) sur la base dudit premier signal de cadencement (112) et de ladite première horloge d'écriture (113) et pour générer également un signal de cadencement de lecture (127) sur la base dudit premier signal de cadencement (112) et d'une horloge de lecture (122) en provenance dudit convertisseur numérique-analogique (121).

FIG.1

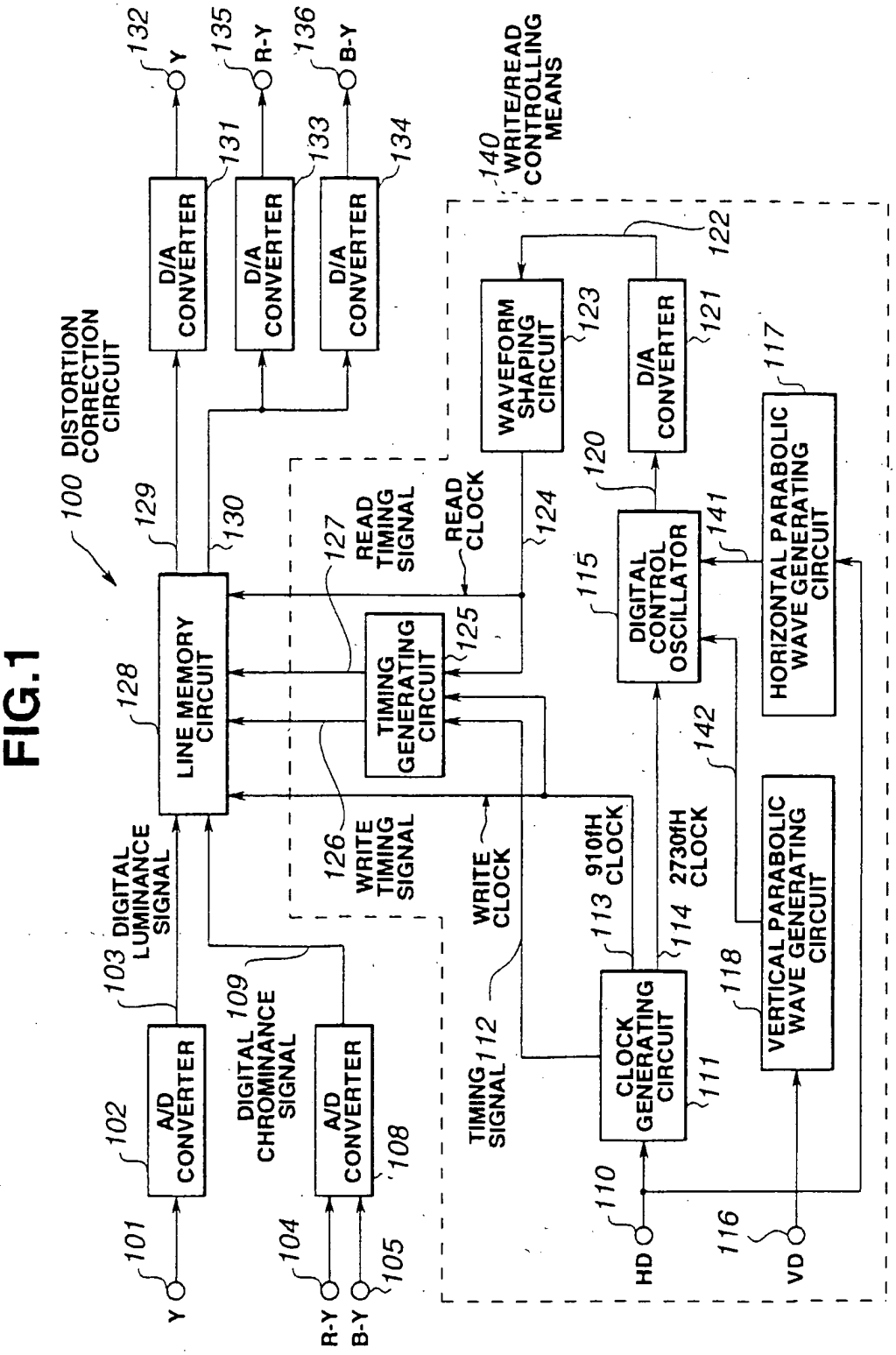
100 DISTORTION CORRECTION CIRCUIT
101 Y
102 A/D CONVERTER
103 DIGITAL LUMINANCE SIGNAL
104 R-Y
105 B-Y
108 A/D CONVERTER
109 DIGITAL CHROMINANCE SIGNAL
110 HD
111 CLOCK GENERATING CIRCUIT
112 TIMING SIGNAL
113 910fH CLOCK
114 2730fH CLOCK
115 DIGITAL CONTROL OSCILLATOR
116 VD
117 HORIZONTAL PARABOLIC WAVE GENERATING CIRCUIT
118 VERTICAL PARABOLIC WAVE GENERATING CIRCUIT
120 D/A CONVERTER
121 D/A CONVERTER
122
123 WAVEFORM SHAPING CIRCUIT
124 READ CLOCK
125 TIMING GENERATING CIRCUIT
126 WRITE TIMING SIGNAL
127 READ TIMING SIGNAL
128 LINE MEMORY CIRCUIT
129
130
131 D/A CONVERTER
132 Y
133 D/A CONVERTER
134 D/A CONVERTER
135 R-Y
136 B-Y
140 WRITE/READ CONTROLLING MEANS
141
142
WRITE CLOCK

FIG.2

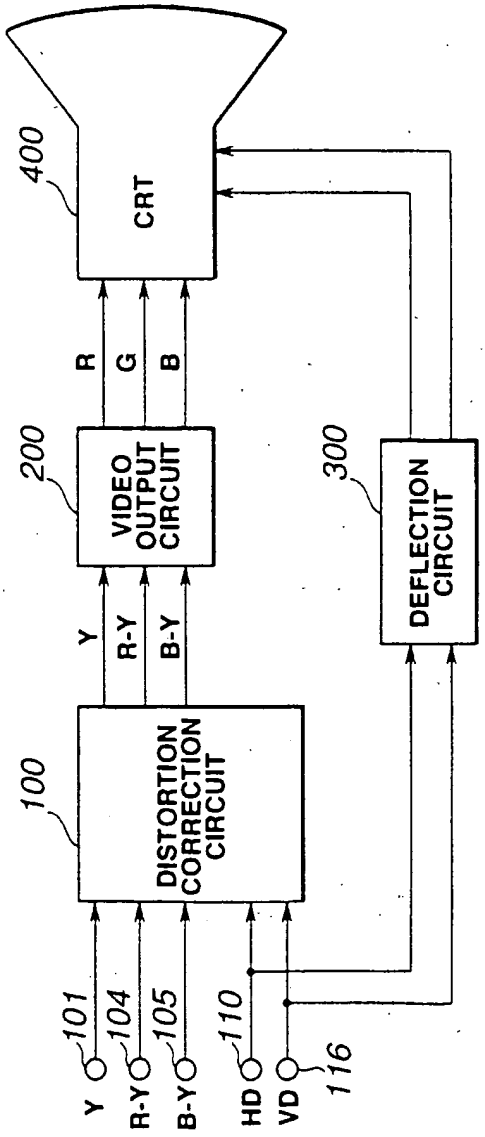
400
CRT
R
G
B
200
VIDEO OUTPUT CIRCUIT
300
DEFLECTION CIRCUIT
Y
R-Y
B-Y
100
DISTORTION CORRECTION CIRCUIT
101
104
105
110
116
Y
R-Y
B-Y
HD
VD

FIG.3(a)

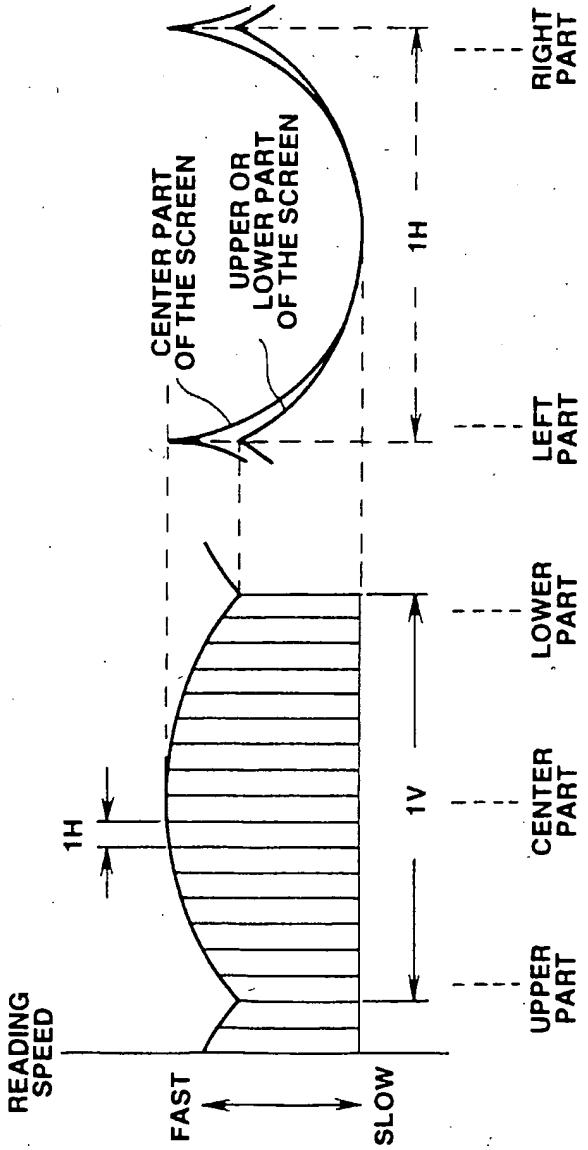
READING SPEED
FAST
SLOW
1H
1V
1H
CENTER PART OF THE SCREEN
UPPER OR LOWER PART OF THE SCREEN
RIGHT PART
LEFT PART
LOWER PART
CENTER PART
UPPER PART

FIG.3(b)

FIG.4(a)

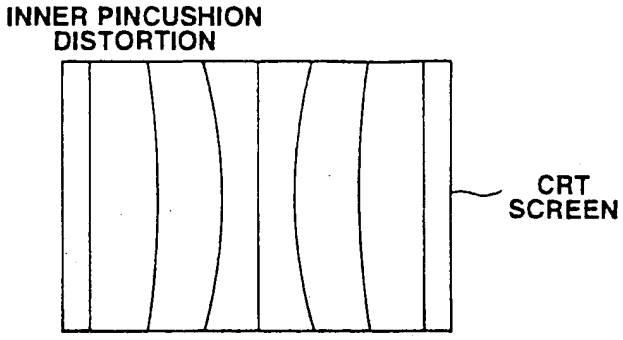

FIG.4(b)

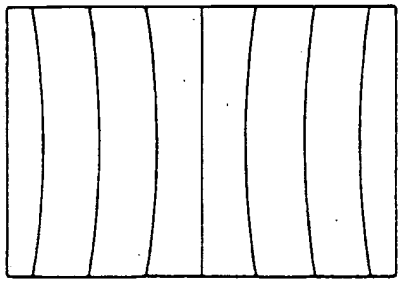

FIG.4(c)

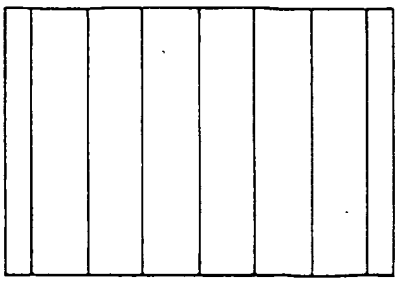

FIG.5(a)

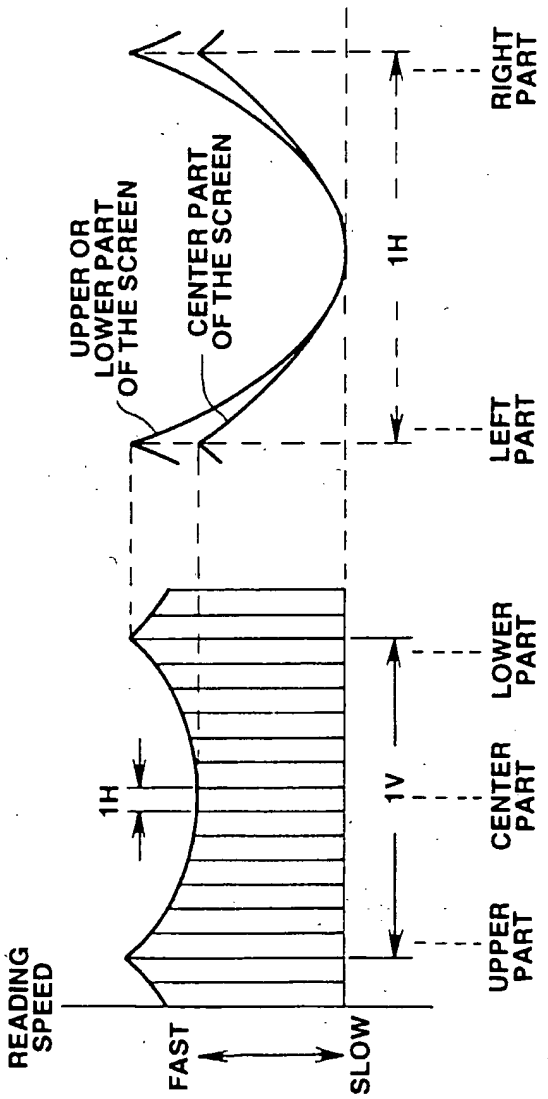
READING SPEED
FAST
SLOW
1H
1V
UPPER PART
CENTER PART
LOWER PART
LEFT PART
1H
RIGHT PART
UPPER OR LOWER PART OF THE SCREEN
CENTER PART OF THE SCREEN

FIG.5(b)

FIG.6(a)

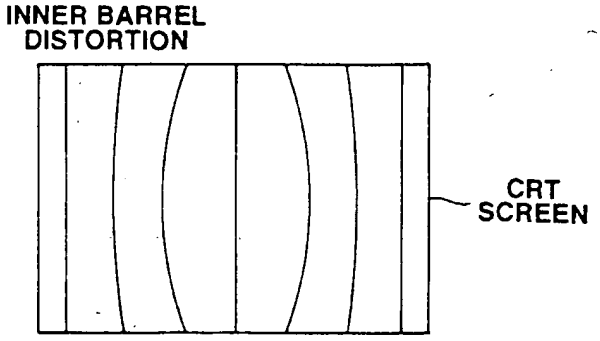

FIG.6(b)

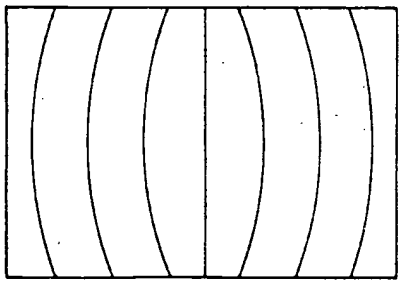

FIG.6(c)

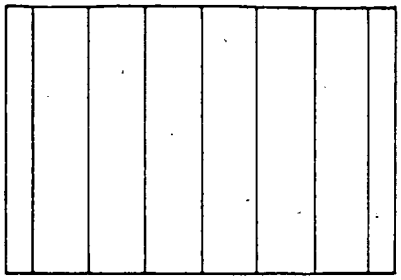

FIG.7
(RELATED ART)

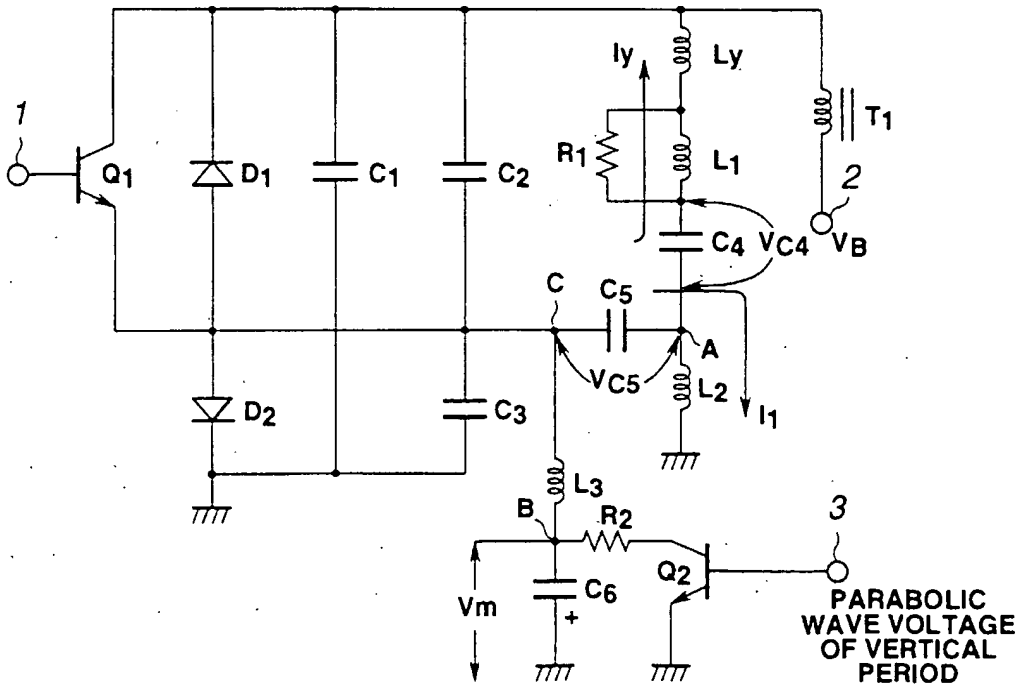

FIG.8
(RELATED ART)

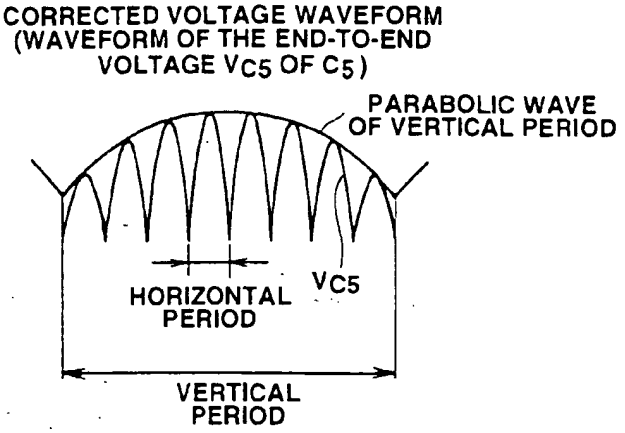

FIG.9(a)
(RELATED ART)

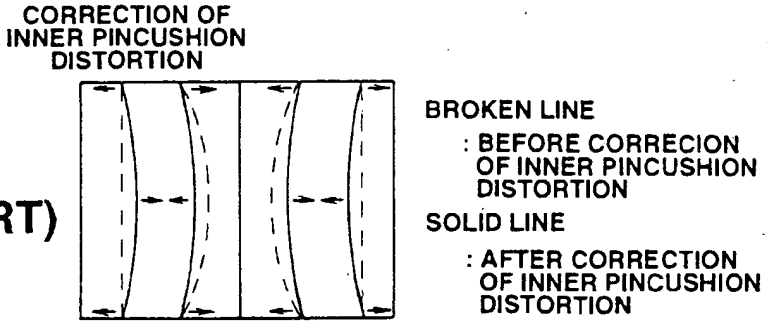

FIG.9(b)
(RELATED ART)

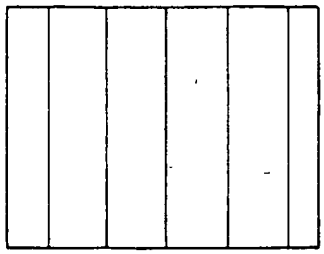

FIG.10
(RELATED ART)